IN THE CLAIMS

1-21. (Cancelled)

22. (New) A method comprising:

forming a device isolation layer in a substrate to define a low voltage region, a high voltage region, and a cell array region therein;

forming a first gate insulating layer on the substrate in the low voltage region;

forming a second gate insulating layer on the substrate in the high voltage region;

forming a first conductive layer overlying the low voltage region and the high voltage region;

forming a triple layer on the substrate in the cell array region, the triple layer including a tunneling insulating layer, a charge storage layer, and a blocking insulating layer; and

forming a second conductive layer on the triple layer.

23. (New) The method of claim 22, further comprising:

forming the first gate insulating layer and the first conductive layer in the cell array region; and

removing the first conductive layer in the cell array region, thereby exposing the substrate in the cell array region.

24. (New) The method of claim 22, wherein the second gate insulating layer is thicker than the first gate insulating layer.

25. (New) A method comprising:

forming a device isolation layer in a substrate to define a high voltage region, a low voltage region, and a cell array region therein;

forming a first gate insulating layer on the substrate in the low voltage region;

forming a second gate insulating layer on the substrate in the high voltage region;

forming a first conductive layer on the first gate insulating layer and the second gate insulating layer;

forming a triple layer on the first conductive layer and the substrate in the cell array region, the triple layer including a tunneling insulation layer, a charge storage layer, and a blocking insulation layer;

forming a second conductive layer on the triple layer;

patterning the second conductive layer, the triple layer, the first conductive layer, the first gate insulating layer, and the second gate insulating layer to form a second gate pattern in the high voltage region, a first gate pattern in the low voltage region;

patterning the second conductive layer, the triple layer to form a cell gate pattern in the cell array region;

removing portions of the second conductive layer and the triple layer from the second gate pattern and from the first gate pattern to form butting regions that expose portions of the first conductive layer;

forming an interlayer insulating layer overlying the resulting structure;

patterning the interlayer insulating layer to form contact holes that expose portions of the butting regions; and

filling the contact holes with contact plugs.

26. (New) The method of claim 25, further comprising:

forming the first gate insulating layer and the first conductive layer in the cell array region; and

removing the first conductive layer in the cell array region, thereby exposing the substrate in the cell array region.

27. (New) The method of claim 25, wherein the substrate further includes a resistor region, the method further comprising:

forming the second gate insulating layer, the first conductive layer, the triple layer, and the second conductive layer on the resistor region;

patterning the second conductive layer, the triple layer, the first conductive layer, and the second gate insulating layer, thereby forming a resistor pattern in the resistor region;

removing the second conductive layer and the triple layer from the resistor pattern; forming the interlayer insulating layer on the resistor pattern and

forming a contact hole exposing a portion of the first conducive layer by patterning the interlayer insulating layer.

28. (New) The method of claim 25, further comprising forming insulating spacers on sidewalls of the second gate patterns, the first gate patterns, and the cell gate patterns.

29. (New) The method of claim 25, wherein forming the second conductive layer comprises stacking a conductive silicon layer and a conductive metal layer.

30. (New) The method of claim 25, wherein the second gate insulating layer is thicker than the first gate insulating layer.

31. (New) A method comprising:

providing a substrate that includes a low voltage region, a high voltage region, and a cell array region;

forming a first gate insulating layer in the low voltage region;

forming a second gate insulating layer in the high voltage region;

forming a first conductive layer on a first gate insulating layer and the second insulating layer;

forming a triple layer over the substrate where the first conductive layer formed, the triple layer including a tunneling insulating layer, a charge storage layer, and a blocking insulating layer;

forming a second conductive layer over the triple layer;

forming a trench type device isolation layer in the substrate to isolate the low voltage region, the high voltage region, and the cell array region from each other;

forming a high conductivity layer over the resulting structure;

patterning the high conductivity layer, the second conductive layer, the triple layer, the second gate insulating layer, and the first gate insulating layer to form a second gate pattern in the high voltage region and a first gate pattern in the low voltage region;

patterning the high conductivity layer, the second conductive layer, and the triple layer to form a cell gate pattern in the cell array region;

removing portions of the high conductivity layer, the second conductive layer, and the triple layer from the second gate pattern and the first gate pattern to form a butting region that exposes the first conductive layer;

forming an interlayer insulating layer over the resulting structure;

patterning the interlayer insulating layer to form contact holes that expose portions of the butting regions; and

filling the contact holes with contact plugs.

32. (New) The method of claim 31, further comprising:

forming the first gate insulating layer and the first conductive layer in the cell array region; and

removing the first conductive layer in the cell array region, thereby exposing the substrate in the cell array region.

33. (New) The method of claim 31, wherein the substrate further includes a resistor region, the method further comprising:

forming the second gate insulating layer, the first conductive layer, the triple layer, the second conductive layer, and the high-conductivity layer in the resistor region,

patterning the resulting structure, thereby forming a resistor pattern in the resistor region;

removing the high-conductivity layer, the second conductive layer, and the triple layer from the resistor pattern;

forming an interlayer insulating layer over the resistor pattern; and

forming a contact hole in the interlayer insulating layer to extend over only the resistor pattern.

34. (New) The method of claim 31, further comprising forming insulating spacers on sidewalls of first gate pattern, the second gate pattern, and the cell gate pattern.

35. (New) The method of claim 31, wherein forming the high conductivity layer comprises sequentially stacking a conductive silicon layer and a conductive metal layer.

36. (New) A method comprising:

forming a device isolation layer on a substrate to define a low voltage region, a high voltage region, and a cell array region;

forming a first gate insulating layer on the substrate in the low voltage region;

forming a second gate insulating layer on the substrate in the high voltage region;

forming a first conductive layer over the first gate insulating layer in the low voltage region and the second gate insulating layer in the high voltage region;

forming a triple layer on the substrate of the cell array region and on the first conductive layer, the triple layer including a tunneling insulation layer, a charge storage layer, and a blocking insulation layer;

forming a second conductive layer on the triple layer;

removing the second conductive layer and the triple layer from the low voltage region and the high voltage region;

forming a high conductivity layer on the first conductive layer in the low voltage region and in the high voltage region, and on the second conductive layer in the cell array region; and

patterning the high conductivity layer, the first conductive layer, the first gate insulation layer, and the second gate insulation layer to form a first gate pattern in the low voltage region and a second gate pattern in the high voltage region; and

patterning the high conductivity layer, the second conductive layer, and the triple layer to form a cell gate pattern in the cell array region.

37. (New) The method of claim 36, further comprising:

forming the first gate insulating layer and the first conductive layer in the cell array region; and

removing the first conductive layer in the cell array region, thereby exposing the substrate in the cell array region.

38. (New) The method of claim 36, further comprising:

forming an interlayer insulating layer over the cell gate pattern, the first gate pattern, and the second gate pattern;

patterning the interlayer insulating layer to form contact holes that expose a portion of the high conductivity layer in each of the cell gate pattern, the first gate pattern, and the second gate pattern; and

filling the contact holes with contact plugs.

39. (New) The method of claim 36, wherein the substrate further includes a resistor region, the method further comprising:

forming the second gate insulating layer, the first conductive layer, the triple layer, the second conductive layer, and the high-conductivity layer in the resistor region;

patterning the resulting structure, thereby forming a resistor pattern in the resistor region;

removing the high conductivity layer, the second conductive layer, and the triple layer from the resistor pattern to expose the first conductive layer of the resistor pattern;

forming the interlayer insulating layer over the first conductive layer of the resistor pattern; and

forming a contact hole through the interlayer insulating layer that extends only over the resistor pattern.

40. (New) A method comprising:

providing a substrate that includes a low voltage region, a high voltage region, and a cell array region;

forming a first gate insulating layer in the low voltage region;

forming a second gate insulating layer in the high voltage region;

forming a first conductive layer on the first gate insulating layer and second gate insulating layer;

forming a triple layer on the substrate of the cell array region and on the first conductive layer, the triple layer including a tunneling insulating layer, a charge storage layer, and a blocking insulating layer;

forming a second conductive layer on the triple layer;

removing the second conductive layer and the triple layer from the low voltage region and the high voltage region;

forming a trench type device isolation layer to isolate the low voltage region, the high voltage region, and the cell array region from each other;

forming a high conductivity layer over the resulting structure;

patterning the high conductivity layer and second conductive layer, and the triple layer to form a cell gate pattern in the cell array region,

patterning the high conductive layer, the first conductive layer, the first gate insulating layer, the second insulating layer to form a first gate pattern in the low voltage region, and to form a second gate pattern in the high voltage region;

forming an interlayer insulating layer over the resulting structure;

patterning the interlayer insulating layer to form contact holes that expose a portion of the high conductivity layer of each of the cell gate pattern, the first gate pattern, and the second gate pattern; and

filling the contact holes with contact plugs.

41. (New) The method of claim 40, further comprising:

forming the first gate insulating layer and the first conductive layer in the cell array region;

removing the first conductive layer in the cell array region, thereby exposing the substrate in the cell array region.

42. (New) The method of claim 40, wherein the substrate further includes a resistor region, the method further comprising:

forming the second gate insulating layer in the resistor region;

forming the second gate insulating layer, the first conductive layer, the triple layer, the second conductive layer, and the high-conductivity layer in the resistor region,

patterning the resulting structure, thereby forming a resistor pattern in the resistor region;

removing the high conductivity layer, the second conductive layer, and the triple layer from the resistor pattern to expose the first conductive layer of the resistor pattern;

forming the interlayer insulating layer over the first conductive layer of the resistor pattern; and

forming a contact hole that exposes only the resistor pattern.

43. (New) The method of claim 40, further comprising forming insulating spacers on sidewalls of the cell gate pattern, the first gate pattern, and the second gate pattern.

44. (New) The method of claim 40, wherein forming the high conductivity layer comprises sequentially stacking a conductive silicon layer and a conductive metal layer.